In the Specification:

Please substitute the below paragraph for the paragraph beginning at page 12, line 24:

– For example, the result of this gating operation could be used alone or in combination with other control signals to generate a gate signal (GATE). This gate signal GATE can be used to turn on pass transistors that transfer write data from the second bypass latch **36b** to the second sense amplifier **34b** outputs. This transfer will overwrite the old read data present at the outputs, but will not interfere with the initial capture of that read data by the second sense amplifier **34b**. Accordingly, if the sense amplifier stage **80** of FIG. 6 is utilized as a final stage within the first and second sense amplifiers **34a, 34b, [[36a, 36b,]]** then the gate signal GATE can be used to transfer write data (shown as BYPASS and /BYPASS) from a bypass latch onto a pair of differential signal lines, while the active low latch enable signal /LE is inactive. This transfer results in an overwrite of the read data provided to the differential signal lines while the latch enable signal /LE is active. This read data may be provided to the differential signal lines during a read operation by driving a sense amplifier control signal line ($CONTROL_{SE}$) high so that complementary read data (READ, /READ) can be passed from an earlier stage of the sense amplifier to the final stage **80**. The illustrated sense amplifier stage **80** comprises a pair of cross-coupled PMOS transistors P1 and P2, a pair of cross-coupled NMOS transistors N3 and N4, a pair of NMOS pull-down transistors N1 and N2 that are responsive to the latch enable signal /LE and a pair of weak load transistors P3 and P4 that are also responsive to the latch enable signal /LE. A first pair of NMOS access transistors N7 and N8 are provided as a pair of switches that control the transfer of bypassed write data to the illustrated pair of differential signal lines, in response to the gate signal GATE. Similarly, a second pair of NMOS access transistors N5 and N6 are provided as a pair of switches that control the transfer of read data to the illustrated pair of differential signal lines, in response to the control signal $CONTROL_{SE}$. –